ST9035
8/16 BIT MCU

DATASHEET

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ST9035

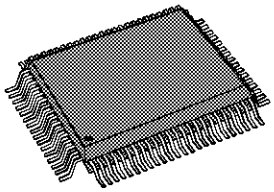
SGS-THOMSON MICROELECTRONICS

ST9035

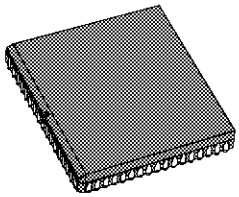
32K ROM HCMOS MCU WITH RAM AND A/D CONVERTER

PRELIMINARY DATA

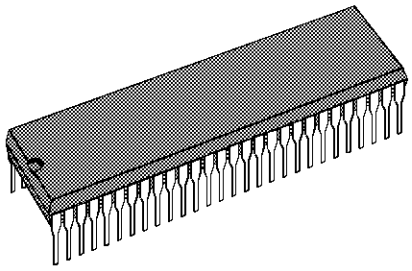
- Register oriented 8/16 bit CORE with RUN, WFI and HALT/SLOW modes
- Minimum instruction cycle time : 500ns (12MHz internal)
- Internal Memory :
  ROM 32K bytes
  RAM 2048 bytes
  224 general purpose registers available as RAM, accumulators or index registers (register file)
- 80-pin PQFP package for ST9035Q
- 68-lead PLCC package for ST9035C
- 56-pin shrink DIP package for ST9035B
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 56 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed and One Time Programmable EPROM parts available for prototyping and pre-production development phases
- Pin to pin compatible with ST9030, ST9036 and ST9040



PQFP80



PLCC68



PSDIP56

(Ordering Information at the end of the Datasheet)

Figure 1. 80 Pin PQFP Package

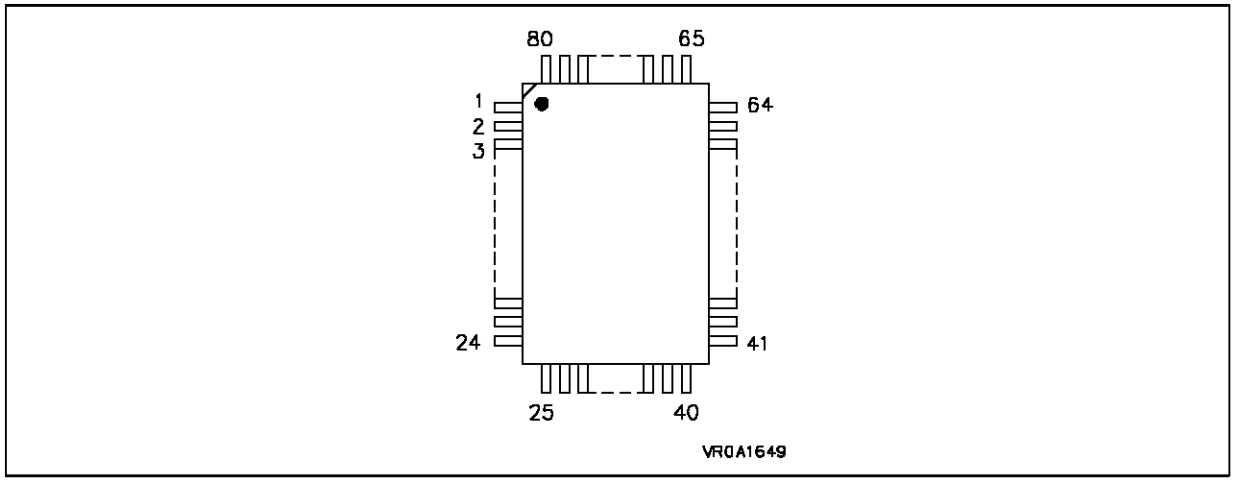


Table 1. ST9035Q Pin Description

Pin	Name
1	AV_{SS}
2	AV_{SS}
3	NC
4	P44/AIN4
5	P57
6	P56
7	P55
8	P54
9	INT7
10	INT0
11	P53
12	NC
13	P52
14	P51
15	P50
16	OSCOUT
17	V_{SS}
18	V_{SS}
19	NC
20	OSCIN
21	$\overline{RESET}$
22	P37/T1OUTB
23	P36/T1INB
24	P35/T1OUTA

Pin	Name
25	P34/T1INA
26	P33/T0OUTB
27	P32/T0INB
28	P31/T0OUTA
29	P30/P/$\overline{D}$/T0INA
30	A15
31	A14
32	NC
33	A13
34	A12
35	A11
36	A10
37	A9
38	A8
39	P00/A0/D0
40	P01/A1/D1

Pin	Name
64	P20/NMI
63	NC
62	V_{SS}
61	P70/SIN
60	P71/SOUT
59	P72/INT4/TXCLK /CLKOUT
58	P73/INT5 /RXCLK/ADTRG
57	P74/P/$\overline{D}$/INT6
56	P75/$\overline{WAIT}$
55	P76/WDOUT /$\overline{BUSREQ}$
54	P77/WDIN /$\overline{BUSACK}$
53	R/$\overline{W}$
52	NC
51	$\overline{DS}$
50	$\overline{AS}$
49	NC
48	V_{DD}
47	V_{DD}
46	P07/A7/D7
45	P06/A6/D6
44	P05/A5/D5
43	P04/A4/D4
42	P03/A3/D3
41	P02/A2/D2

Pin	Name
80	AV_{DD}
79	NC
78	P47/AIN7
77	P46/AIN6
76	P45/AIN5
75	P43/AIN3
74	P42/AIN2
73	P41/AIN1
72	P40/AIN0
71	P27/RRDY5
70	P26/INT3 /$\overline{RDSTB}$5/P/$\overline{D}$
69	P25/WRRDY5
68	P24/INT1 /$\overline{WRSTB}$5
67	P23/SDO
66	P22/INT2/SCK
65	P21/SDI/P/$\overline{D}$

Figure 2. 68 Pin PLCC Package

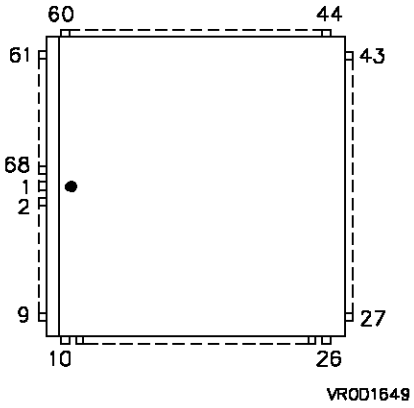


Table 2. ST9035C Pin Description

Pin	Name
61	P44/AIN4
62	P57
63	P56
64	P55
65	P54
66	INT7
67	INT0
68	P53
● 1	P52
2	P51
3	P50
4	OSCOUT
5	V_{SS}
6	OSCIN
7	$\overline{\text{RESET}}$
8	P37/T1OUTB
9	P36/T1INB

Pin	Name
10	P35/T1OUTA
11	P34/T1INA
12	P33/T0OUTB
13	P32/T0INB
14	P31/T0OUTA
15	P30/P/$\overline{\text{D}}$/T0INA
16	P17/A15
17	P16/A14
18	P15/A13
19	P14/A12
20	P13/A11
21	P12/A10
22	P11/A9
23	P10/A8
24	P00/A0/D0
25	P01/A1/D1
26	P02/A2/D2

Pin	Name
43	P70/SIN
42	P71/SOUT
41	P72/CLKOUT /TXCLK/INT4
40	P73/ADTRG /RXCLK/INT5
39	P74/P/$\overline{\text{D}}$/INT6
38	$\overline{\text{P75/WAIT}}$
37	P76/WDOUT /$\overline{\text{BUSREQ}}$
36	P77/WDIN /$\overline{\text{BUSACK}}$
35	R/$\overline{\text{W}}$
34	$\overline{\text{DS}}$
33	$\overline{\text{AS}}$
32	V_{DD}
31	P07/A7/D7
30	P06/A6/D6
29	P05/A5/D5
28	P04/A4/D4
27	P03/A3/D3

Pin	Name
60	AV_{SS}
59	AV_{DD}
58	P47/AIN7
57	P46/AIN6
56	P45/AIN5
55	P43/AIN3
54	P42/AIN2
53	P41/AIN1
52	P40/AIN0
51	P27/RRDY5
50	P26/INT3 /$\overline{\text{RDSTB5}}$/P/$\overline{\text{D}}$
49	P25/WRRDY5
48	P24/INT1 /$\overline{\text{WRSTB5}}$
47	P23/SDO
46	P22/INT2/SCK
45	P21/SDI/P/$\overline{\text{D}}$
44	P20/NMI

Figure 1b. 56 Pin Shrink DIP Pinout

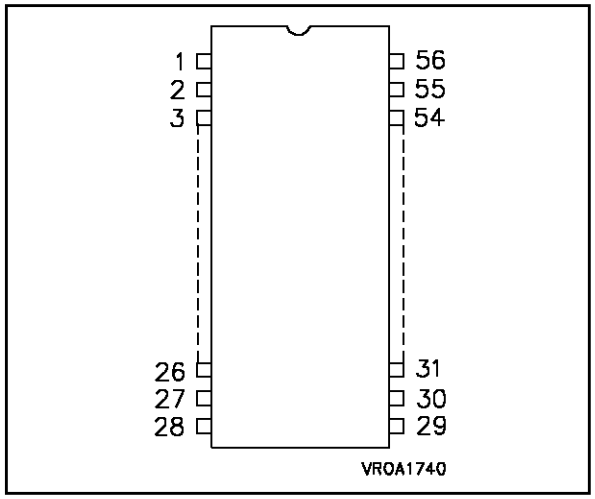


Table 3. ST9035B Pin Description

Pin	Pin name
1	P42/AIN2
2	P43/AIN3
3	P45/AIN5
4	P46/AIN6
5	P47/AIN7
6	AVDD
7	AVSS
8	P44/AIN4
9	P57
10	P56
11	P55
12	P54
13	P53
14	P52
15	OSCOUT
16	V_{SS}
17	OSCIN
18	$\overline{\text{RESET}}$
19	P37/T1OUTB
20	P36/T1INB
21	NC
22	P35/T1OUTA
23	P34/T1INA
24	P33/T0OUTB
25	P32/T0INB
26	P31/T0OUTA
27	P30/P/D/T0INA
28	P13/A11

Pin	Pin name
56	P41/AIN1
55	P40/AIN0
54	P23/SDO
53	P22/INT2/SCK
52	P21/SDI/P/$\overline{\text{D}}$
51	P20/NMI
50	P70/SIN
49	P71/SOUT
48	P72/CLKOUT TXCLK/INT4
47	P73/ADTRG RXCLK/INT5
46	P76/WDOUT/$\overline{\text{BUSREQ}}$
45	P77/WDIN/BUSACK
44	R/$\overline{\text{W}}$
43	DS
42	$\overline{\text{AS}}$
41	V_{DD}
40	V_{SS}
39	P07/A7/D7
38	P06/A6/D6
37	P05/A5/D5
36	P04/A4/D4
35	P03/A3/D3
34	P02/A2/D2
33	P01/A1/D1
32	P00/A0/D0
31	P10/A8
30	P11/A9
29	P12/A10

1.1 GENERAL DESCRIPTION

The ST9035 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ST9035 EPROM peripheral and functional actions are fully compatible throughout the ST903x/4x family. This datasheet will thus provide only information specific to this ROM device.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9030 ROM-BASED DEVICE FOR FURTHER DETAILS.

The nucleus of the ST9035 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set. The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9035 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.
Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer. In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375,000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

1.2 PIN DESCRIPTION

$\overline{AS}$. Address Strobe (output, active low, 3-state). Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

DS. Data Strobe (output, active low, 3-state). Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of **$\overline{DS}$**. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST9035 accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. Read/Write (output, 3-state). Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. Reset (input, active low). The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

INT0, INT7. External interrupts (input, active on rising or falling edge). External interrupt inputs 0 and 7 respectively. INT0 channel may also be used for the timer watchdog interrupt.

OSCIN, OSCOUT. Oscillator (input and output). These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter. Must be tied to V_{SS}.

V_{DD}. Main Power Supply Voltage (5V ± 10%)

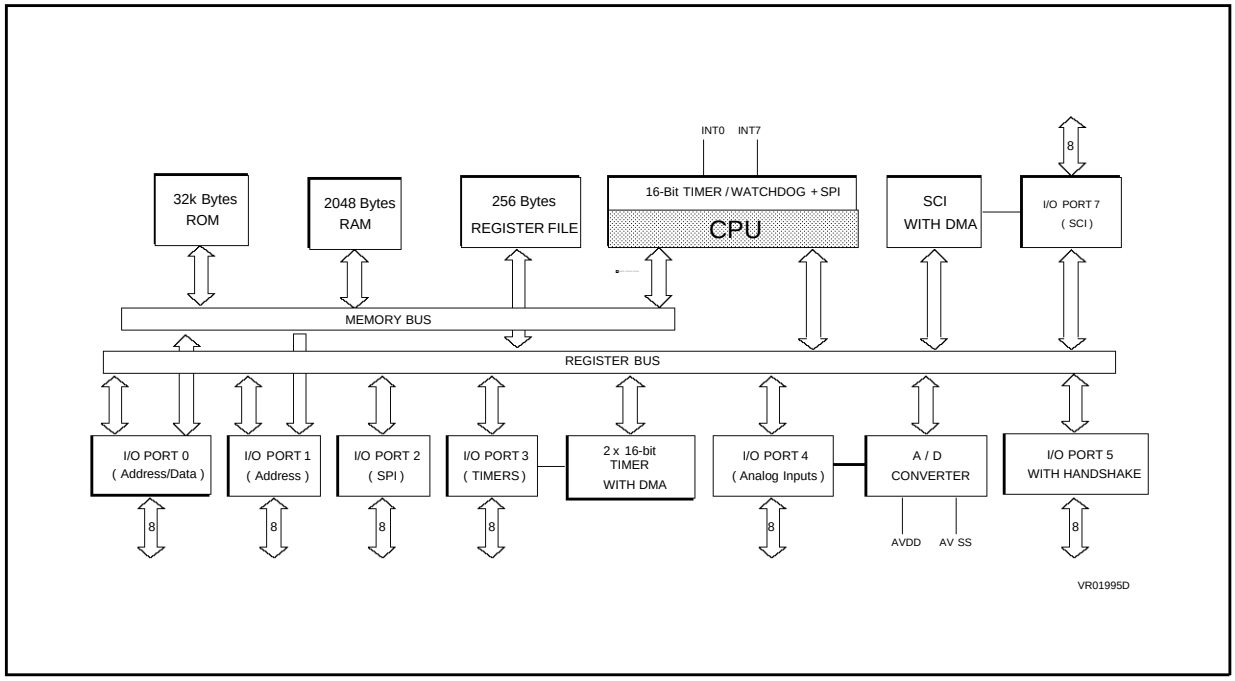
V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 I/O Port Lines (Input/Output, TTL or CMOS compatible). 56 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as alternate functions.

1.2.1 I/O Port Alternate Functions

Each pin of the I/O ports of the ST9035 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Table 1-4 shows the Functions allocated to each I/O Port pins and a summary of packages for which they are available.

Figure 3. ST9035 Block Diagram



PIN DESCRIPTION (Continued)

Table 4. ST9035 I/O Port Alternate Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment		
Port. bit				PLCC	PQFP	PSDIP
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24	39	32
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25	40	33
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26	41	34
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27	42	35
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28	43	36
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29	44	37
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30	45	38
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31	46	39
P1.0	A8	O	Address bit 8	23	38	31
P1.1	A9	O	Address bit 9	22	37	30
P1.2	A10	O	Address bit 10	21	36	29
P1.3	A11	O	Address bit 11	20	35	28
P1.4	A12	O	Address bit 12	19	34	
P1.5	A13	O	Address bit 13	18	33	
P1.6	A14	O	Address bit 14	17	31	
P1.7	A15	O	Address bit 15	16	30	
P2.0	NMI	I	Non-Maskable Interrupt	44	64	51
P2.0	ROMless	I	ROMless Select (Mask option)	44	64	51
P2.1	P/$\overline{D}$	O	Program/Data Space Select	45	65	
P2.1	SDI	I	SPI Serial Data Out	45	65	52
P2.2	INT2	I	External Interrupt 2	46	66	53
P2.2	SCK	O	SPI Serial Clock	46	66	53
P2.3	SDO	O	SPI Serial Data In	47	67	54
P2.4	INT1	I	External Interrupt 1	48	68	
P2.4	$\overline{WRSTB5}$	I	Handshake Write Strobe P5	48	68	
P2.5	WRRDY5	O	Handshake Write Ready P5	49	69	
P2.6	INT3	I	External Interrupt 3	50	70	
P2.6	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	50	70	
P2.6	P/$\overline{D}$	O	Program/Data Space Select	50	70	
P2.7	RDRDY5	O	Handshake Read Ready P5	51	71	
P3.0	T0INA	I	MF Timer 0 Input A	15	29	27
P3.0	P/$\overline{D}$	O	Program/Data Space Select	15	29	27
P3.1	T0OUTA	O	MF Timer 0 Output A	14	28	26
P3.2	T0INB	I	MF Timer 0 Input B	13	27	25
P3.3	T0OUTB	O	MF Timer 0 Output B	12	26	24
P3.4	T1INA	I	MF Timer 1 Input A	11	25	23

PIN DESCRIPTION (Continued)

Table 4. ST9035 I/O Port Alternate Function Summary(Continued)

I/O PORT	Name	Function	Alternate Function	Pin Assignment		
Port. bit				PLCC	PQFP	PSDIP
P3.5	T1OUTA	O	MF Timer 1 Output A	10	24	22
P3.6	T1INB	I	MF Timer 1 Input B	9	23	20
P3.7	T1OUTB	O	MF Timer 1 Output B	8	22	19
P4.0	AIN0	I	A/D Analog Input 0	52	72	55
P4.1	AIN1	I	A/D Analog Input 1	53	73	56
P4.2	AIN2	I	A/D Analog Input 2	54	74	1
P4.3	AIN3	I	A/D Analog Input 3	55	75	2
P4.4	AIN4	I	A/D Analog Input 4	61	4	8
P4.5	AIN5	I	A/D Analog Input 5	56	76	3
P4.6	AIN6	I	A/D Analog Input 6	57	77	4
P4.7	AIN7	I	A/D Analog Input 7	58	78	5
P5.0		I/O	I/O Handshake Port 5	3	15	
P5.1		I/O	I/O Handshake Port 5	2	14	
P5.2		I/O	I/O Handshake Port 5	1	13	14
P5.3		I/O	I/O Handshake Port 5	68	11	13
P5.4		I/O	I/O Handshake Port 5	65	8	12
P5.5		I/O	I/O Handshake Port 5	64	7	11
P5.6		I/O	I/O Handshake Port 5	63	6	10
P5.7		I/O	I/O Handshake Port 5	62	5	9
P7.0	SIN	I	SCI Serial Input	43	61	50
P7.1	SOUT	O	SCI Serial Output	42	60	49
P7.1	ROMless	I	ROMless Select (Mask option)	42	60	49
P7.2	INT4	I	External Interrupt 4	41	59	48
P7.2	TXCLK	I	SCI Transmit Clock Input	41	59	48
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41	59	48
P7.3	INT5	I	External Interrupt 5	40	58	47
P7.3	RXCLK	I	SCI Receive Clock Input	40	58	47
P7.3	ADTRG	I	A/D Conversion Trigger	40	58	47
P7.4	INT6	I	External Interrupt 6	39	57	
P7.4	P/$\overline{D}$	O	Program/Data Space Select	39	57	
P7.5	$\overline{WAIT}$	I	External Wait Input	38	56	
P7.6	WDOUT	O	T/WD Output	37	55	46
P7.6	$\overline{BUSREQ}$	I	External Bus Request	37	55	46
P7.7	WDIN	I	T/WD Input	36	54	45
P7.7	$\overline{BUSACK}$	O	External Bus Acknowledge	36	54	45